PTO/SB/08A (06-03)

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INFO	STATEMENT BY APPLICANT			Filing Date			
STA				First Named Inventor	Pan, Phillip		
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(use as many sheets as necessary)			ecessary)	Examiner Name			
Sheet	1	of	2	Attorney Docket Number	015114-054411US		

<u> </u>			U.S. PATENT DO	CUMENIS	
Examiner Initials*	Cite No.1	Document Number Number Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Examiner Initials*	Cite No.1	Foreign Patent Document		FENT DOCUME	Name of Patentee or	Pages, Columns, Lines,	T .	
		Country Code ³	Number ⁴	Kind Cade [®] (# known)	Publication Date MM-DD-YYYY	Applicant of Cited Document	Where Relevant Passages or Relevant Figures Appear	Τġ
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Substitute for form 1449B/PTO		Complete if Known
INCODMATION BIOOLOGUBE	Application Number	11623394
INFORMATION DISCLOSURE	Filing Date	1000
STATEMENT BY APPLICANT	First Named Inventor	Pan, Phillip
	. Art Unit	
(use as many sheets as necessary)	Examiner Name	
Sheet 2 of 2	Attorney Docket Number	015114-054411US

Examiner Initials	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T 2
AT	ВС	MICHAEL B. BENDAK et al., "CMOS VLSI Implementation of Gigabyte/Second Computer Network Links", IEEE, 1996	
	BD	"Virtex-II 1.5V Field-Programmable Gate Arrays", XILINX, DS031-2 (v1.5), April 2, 2001	
	BE	ANDREA BONI et al., "LVDS i/O Interface for Gb/s-per-Pin Operation in 0.35-μm CMOS" IEEE Journal of Solid-State Circuits, vol. 36, no. 4, April 2001	
	BF	*APEX II Programmable Logic Device Family*, Altera Corporation, May 2001	
	BG	*APEX 20K Programmable Logic Device Family*, Altera Corporation, May 2001	
	вн	LVDS I/O Interface for Gb/s-per-Pin Operation in 0.35-µm CMOS; Boni, et al., IEEE Journal of Solid-State Circuits, Vol. 36, No. 4, April 2001	
	ВІ	CMOS VLSI Implementation of Gigabyte/Second Computer Network Links, Bendak et al., Dept. of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA 92093-0407, IEEE International Symposium on Circuits and Systems, 1996	:
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Complete if Known Substitute for form 1449A/PTO 10/623,394 **Application Number** INFORMATION DISCLOSURE July 18, 2003 Filing Date Pan, Phillip First Named Inventor STATEMENT BY APPLICANT Art Unit

Examiner Name (use as many sheets as necessary) Sheet

015114-054411US **Attorney Docket Number**

			U.S. PATENT DO	CUMENTS+	
		Document Number	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant
xaminer Initials*	Cite No.1	Number Kind Code ² (if known)	MM-DD-YYYY	McCracken et al.	Figures Appear
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+	AB AC	US-6,504,790 B1	01/07/03	Wolford	<u> </u>
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Examiner Initials*	Cite No.1	For	eign Patent Doo		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Where Relevant Passages or Relevant Figures Appear	τ°
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